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Remarks/Arguments

This Response is provided in response to the Advisory Action mailed January 24, 2007, in which the Examiner rejected claims 1-9, 13, and 15-29 under 35 U.S.C. §102(e) as being anticipated over the prior art, and in which the Examiner rejected claims 10-12 and 14 under 35 U.S.C.§103(a) as being obvious in view of the prior art. In view of the present amendments and remarks, the Applicants believe that claims 1-29 are presently in condition for allowance.

Support for amendments to claims 1, 15, 16, and 21

One embodiment of the Applicants' present invention is directed to methods and apparatus for performance measurement of different network routes between devices. *See* e.g., Specification pg. 5, lines 21-22. Typically, a network includes multiple paths between a first and a second device. *See* e.g., Specification pg. 5, lines 22-23. A preferred embodiment of the Applicants' present invention includes a first test of a first type conducted over a first path between a first and second device, and a second test of a first type conducted over a second path between a first and second device simultaneously. *See* e.g., Specification pg. 5, lines 23-25. In preferred and claimed embodiment, a single test signal is applied along two separate paths between a first and second device simultaneously so that comparative data can be derived regarding each of the separate paths. *See* e.g., Specification pg. 5, lines 25-27.

Turning to the claims, independent claims 1, 15, and 16 recite *inter alia*,

> "a processor initiates the simultaneous execution of the first and the second non-sequential performance tests."

Similarly, independent claim 21 recites *inter alia*,

> "a processor initiates the simultaneous execution of a performance test between the first device and the second device over each of the first and second transport networks simultaneously."

Ample support for processor initiated simultaneous testing of a plurality of paths between a first and second device exists in the specification. Examples in the current application include at least two separate means and methods for the simultaneous testing of two network paths.

A first example uses a processor 281 that is described as being connected to network interfaces 284 by means of multiple communication mechanisms 289 to perform one or more tasks or processes. *See* Specification pg. 9, lines 6-11; *See also* Fig. 2B. Based on this description, the processor, for example, can execute a single test instruction (a test execution command for example) and distribute that signal onto two communication mechanisms 289 to deliver the signal to one or more network interfaces 284 for the simultaneous testing of a network paths. Thus, through a processor executing a single command, two tests can be executed simultaneously.

A second example involves a technique that includes using processing loops to queue a test signal until a performance test can be conducted simultaneously. *See* Specification pg. 11, lines 5-11; *See also* Fig. 5B. By using this technique, a first test signal, for example, is issued and queued using a processing loop while a second test signal is executed and sent to the network interface. When the second test signal arrives at the network interface, a simultaneous performance test between first and second devices on two paths is executed simultaneously.

Thus, the Applicants do have a system which allows for processor initiation of a first and second non-sequential performance test to be executed simultaneously on two paths. As stated above, there is at a minimum, two separate ways detailed in the specification to execute the simultaneous testing. The first example detailed a way of testing the paths wherein the processor issues one command and then the command is distributed onto two paths. The second example detailed the processor executing commands one after another then synching the tests through the use of a processing loop to queue the first command until the second command is received whereby simultaneous

testing can be initiated. Thus, the system detailed in independent claims 1, 15, 16, and 21 has the capability to utilize performance tests for the testing of two paths or transport networks simultaneously.

Rejection of Claims Under 35 U.S.C. §102(e)

The Office Action rejected claims 1-9, 13, and 15-29 under 35 U.S.C. §102(e) as being unpatentable over United States Patent No. 6,763,380 issued to Mayton et al., July 13, 2004 (Mayton). The Applicants respectfully traverse this rejection.

Legal Precedent

Anticipation means a lack of novelty, and is a question of fact which is reviewed by the reviewing court using a substantial evidence standard. *Brown v. 3M*, 60 USPQ2d 1375 (Fed. Cir. 2001); *Baxter Int'l, Inc. v. McGaw, Inc.*, 47 USPQ2d 1225 (Fed. Cir. 1998). To anticipate a claim, every limitation of the claim must be found in a single prior art reference, arranged as in the claim. *Karsten Mfg. Corp. v. Cleveland Golf Co.*, 58 USPQ2d 1286 (Fed. Cir. 2001). *Festo Corp. v. Shoketsu Kinzoku Kogyo Kabushiki Co.*, 122 S.Ct. 1831 (2002). Each such limitation must be found either expressly or inherently in the prior art reference. *Schering Corporation v. Geneva Pharmaceuticals, Inc.*, 02-1540, Decided August 1, 2003 (Fed. Cir. 2003). Accordingly, the Applicants need only point to a single element not found in the cited reference to demonstrate that the cited reference fails to anticipate the claimed subject matter.

The cited reference fails to show processor initiated simultaneous execution of the first and the second non-sequential tests over two paths as recited by independent claims 1, 15, 16, and 21.

In explaining how Mayton anticipates independent claims 1, 15, 16, and 21 with respect to simultaneous testing in the Final Office Action dated October 20, 2006, the Examiner stated, "The Examiner must again state that performance tests completed utilizing an extremely short time period are considered to be simultaneous, and that the tests are

performed essentially simultaneously. In addition, performance tests completed utilizing user initiation can be performed essentially simultaneously, since initiation can be performed simultaneously." *See* Final Office Action pg. 4, lines 1-5. To support the first comment above, that is "The Examiner must again state that performance tests completed utilizing an extremely short time period are considered to be simultaneous, and that the tests are performed essentially simultaneously," the Examiner cites Mayton col. 3, lines 22-24. *See* Final Office Action pg. 7, lines 1-4. This section of Mayton states, "Network performance measurements may be obtained on a repeated basis, for example, pursuant to a test schedule."

It is important to note that the currently amended independent claims 1, 15, 16 and 21 include the term non-sequential. While the specification allows for the testing to be either non-sequential (*See* Specification pg. 5, lines 25-27: specifically "simultaneously"), or sequential (*See* Specification pg. 5, lines 25-27: specifically "within a close time proximity"), the current independent claims recite only testing of the devices to be done in a non-sequential (simultaneous) manner. Amended claims 1, 15, 16, and 21 are directed to non-sequential testing, not to periodic scheduled (sequential) testing, as disclosed in Mayton (measurements obtained on a repeated basis). Therefore, the Examiner's statement that "tests completed utilizing an extremely short time period are considered to be simultaneous" is moot due to the amendment of claims 1, 15, 16, and 21 to specifically claim non-sequential testing. Thus, since the language of Mayton specifically states that measurements may be obtained **on a repeated basis**, and a repeated basis necessitates a period of time pass between the measurements, the measurements disclosed in Mayton are necessarily sequential measurements and thus do not anticipate the non-sequential tests of claims 1, 15, 16, and 21.

The current amendments to claims 1, 15, 16, and 21 further claim that a processor initiates the execution of the first and second non-sequential performance test simultaneously on two paths. The Examiner has attempted to rely on Mayton col. 13, lines 30-32 which states in full, "In addition, initiation of traceroute operations may be provided

responsive to a specific user request" to show that a user could initiate a secondary test near a time when a first test was being run. The Examiner has stated, "user initiation **can** be performed essentially simultaneously" (Emphasis added). *See* Office Action pg. 4, line 4. However, this section fails to point out any teaching in Mayton that a processor initiates the simultaneous execution of the tests, and can at best describe a user manually executing a test at a time near a scheduled test execution. Since there is no teaching in Mayton that a processor initiates the simultaneous execution of the tests, Mayton fails to anticipates the limitations of claims 1, 15, 16, and 21.

As described in the text above, there is no showing in the Mayton reference of utilizing a processor to initiate the execution of first and second non-sequential performance tests simultaneously on two paths as claimed in claims 1, 15, 16, and 21. Thus, Mayton fails to anticipate every limitation of independent claims 1, 15, 16, and 21. Furthermore, based at least upon their dependency to claims 1, 16, and 21, claims 2-14, 17-20, and 22-29 are not anticipated by Mayton. For at least these reasons among others, the Applicants respectfully request withdrawal of the rejections under 35 U.S.C. § 102, and passage of claims 1-29 to allowance.

Rejection of Claims Under 35 U.S.C. §103(a)

The Office Action further rejected claims 10, 11, and 14 under 35 U.S.C. §103(a) as being unpatentable over Mayton in view of United States Patent No. 6,360,268 issued to Stephen Silva et al., March 19, 2002 (Silva). This rejection is respectfully traversed.

Legal Precedent

The United States Court of Appeals for the Federal Circuit have provided specific guidance regarding the kind of factual findings needed to determine a reason, suggestion, or motivation to combine references in support of a prima facie showing of unpatentability under 35 U.S.C. §103(a). "The reason, suggestion, or motivation to combine may be found explicitly or implicitly: 1) in the prior art references themselves; 2) in the knowledge of those of ordinary skill in the art that certain references, or disclosures in those references,

are of special interest or importance in the field; or 3) from the nature of the problem to be solved, "leading inventors to look to references relating to possible solutions to that problem." *Pro-Mold & Tool Co. v. Great Lake Plastics, Inc.*, 75 F.3d 1568, 1572, 37 USPQ2d 1626, 1630 (Fed. Cir. 1996) (internal citations omitted); *In re Rouffet*, 149 F.3d at 1357, 47 USPQ2d at 1458. While the references need not expressly teach that the disclosure contained therein should be combined with another, see *Motorola, Inc. v. Interdigital Tech. Corp.*, 121 F.3d 1461, 1472, 43 USPQ2d 1481, 1489(Fed. Cir. 1997), the showing of combinability must be "clear and particular." *In re Dembiczak*, 175 F.3d at 999, 50 USPQ2d at 1617." *Ruiz v. A.B. Chance Co.*, 57 USPQ2d 1161 (Fed. Cir. 2000).

The cited references, taken alone or in combination, fail to teach or suggest features recited by claims 10, 11, and 14.

Claims 10, 11, and 14 depend from independent claim 1, and include all limitations of independent claim 1. As discussed above in the section titled "Rejection of Claims Under 35 U.S.C. §102(e)", Mayton fails to teach or suggest the amended limitations of claim 1. Silva supplies neither the missing elements nor a showing for the combinability of the two references. Thus, neither Mayton nor Silva, taken alone or in combination, teach the above limitations of claim 1. Due to at least the dependencies of claims 10, 11, and 14 on claim 1, the cited references, taken alone or in hypothetical combination, cannot render obvious claims 10, 11, and 14. For at least these reasons, as well as for reasons previously presented, the Applicants request withdrawal of the rejection of claims 10, 11, and 14 under 35 U.S.C. §103(a), and passage of same to allowance.

Rejection of Claims Under 35 U.S.C. §103(a)

The Examiner further rejected claim 12 under 35 U.S.C. §103(a) as being unpatentable over Mayton in view of U.S. Publication No. 2003/0036865, inventor ZhangQing Zhuo et al., February 20, 2003, (Zhuo).

The cited references, taken alone or in combination, fail to teach or suggest features recited by claim 12.

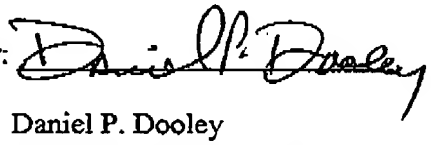
As discussed above in the section titled "Rejection of Claims Under 35 U.S.C. §102(e)", Mayton fails to teach or suggest the amended limitations of claim 1. Zhuo supplies neither the missing elements nor a showing for the combinability of the two references. Thus, neither Mayton nor Zhuo, taken alone or in combination, teach the above recitations of claim 1. Due to at least the dependency of claim 12 on claim 1, the cited references, taken alone or in hypothetical combination, cannot render obvious claim 12. For at least these reasons, as well as for reasons previously presented, the Applicants request withdrawal of the rejection of claim 12 under 35 U.S.C. §103(a), and passage of same to allowance.

Conclusion

The Applicants respectfully submit that all pending claims should be in condition for allowance. This Response is intended to be a complete response to the Advisory Action mailed January 24, 2007.

However, if the Examiner believes certain amendments are necessary to clarify the present claims or if the Examiner wishes to resolve any other issues by way of a telephone conference, the Examiner is kindly invited to contact the undersigned attorney at the telephone number indicated below.

Respectfully submitted,

By: 

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